HARD MACRO HAVING IMPROVED PORT ROUTING

ABSTRACT OF THE DISCLOSURE

Disclosed is an improved hard macro design for use in an ASIC, which avoids undesirable buildup of electrostatic charge on a gate of an I/O transistor of the hard macro. The hard macro includes a port level metallic conductor of an I/O port positioned at a low level metalization layer and an electrical connection between the port level metallic conductor and a gate conductor of the I/O transistor. The electrical connection includes a first conducting section extending from the gate conductor to a top level metallic conductor at a highest level metalization layer and a second conducting section extending from the top level metallic conductor layer to the port level conductor. Antenna rule violations at the I/O port of the hard macro are eliminated due to the electrical connection between the top level metallic conductor and a diffusion region.